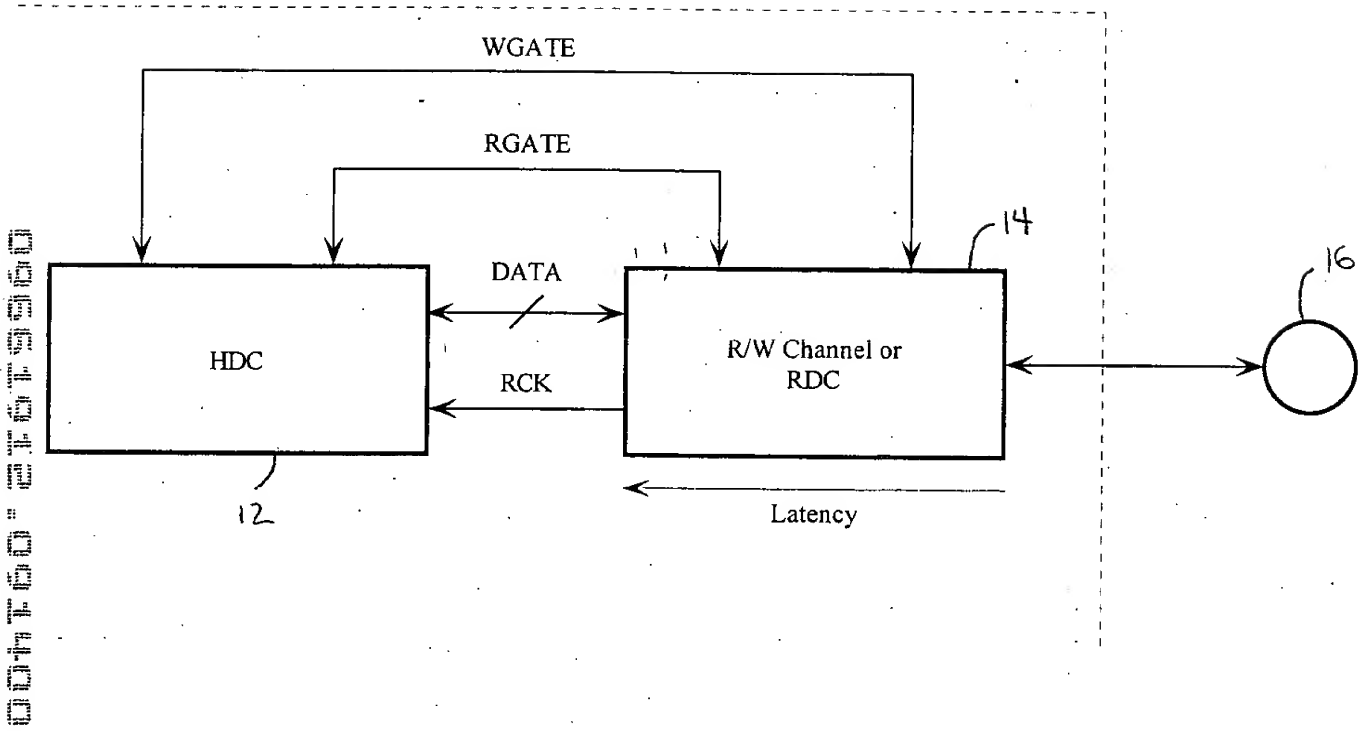

Fig. 1

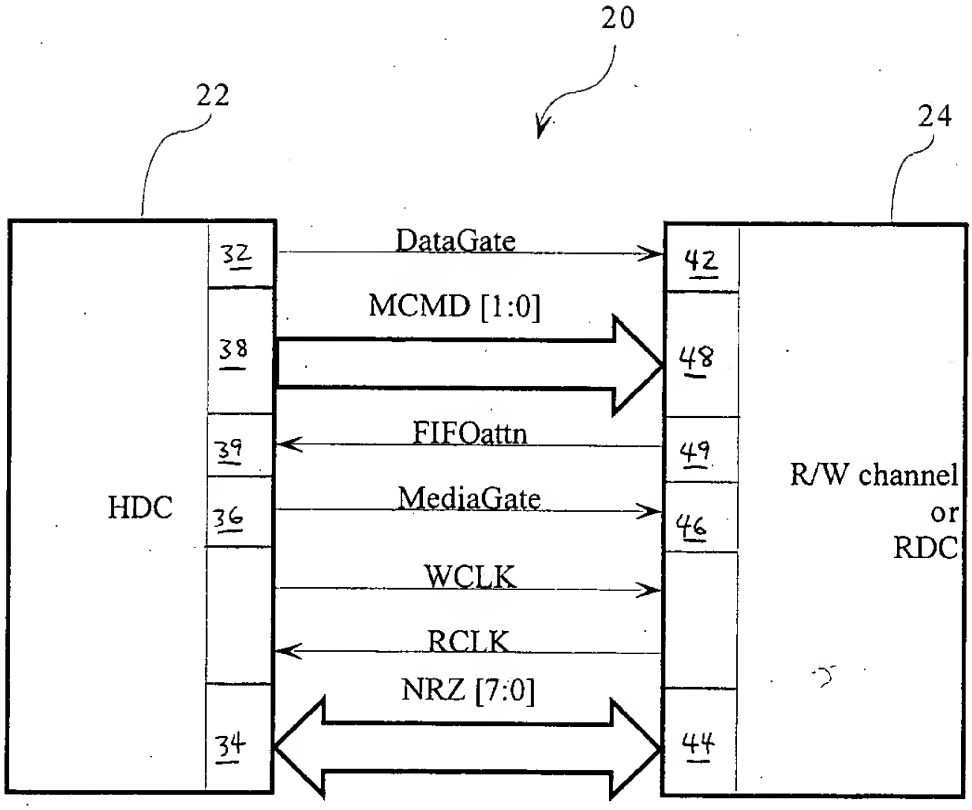
20
22
24
HDC
32
38
39
36
34
DataGate
MCMD [1:0]
FIFOattn
MediaGate
WCLK
RCLK
NRZ [7:0]
42
48
49
46
44
R/W channel
or
RDC

Fig. 2

MV Interface Description
This interface uses additional pins to provide Tag/mode selection info for future implementations of high latency RDC designs with latency could be more than one sector long

MCMD timing chart for Write/Read operations

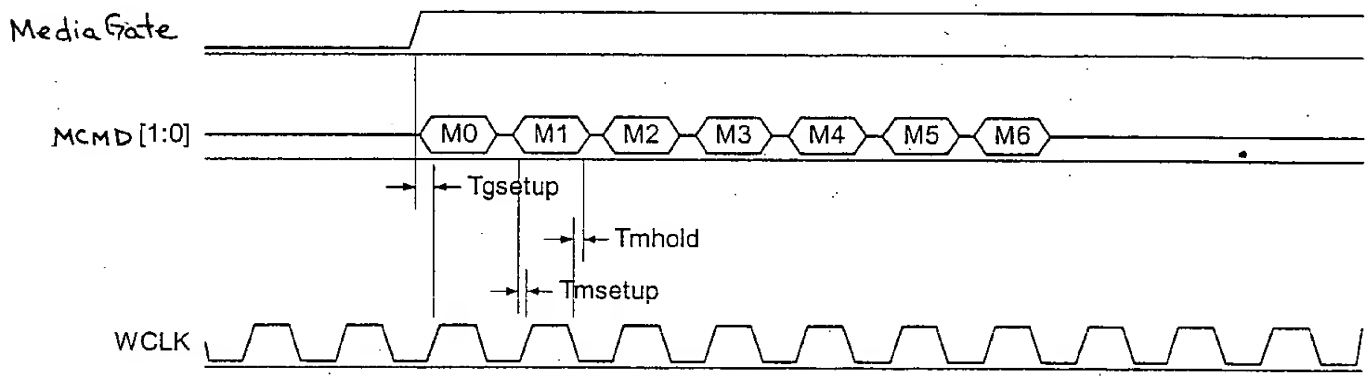

Fig. 3

High latency write

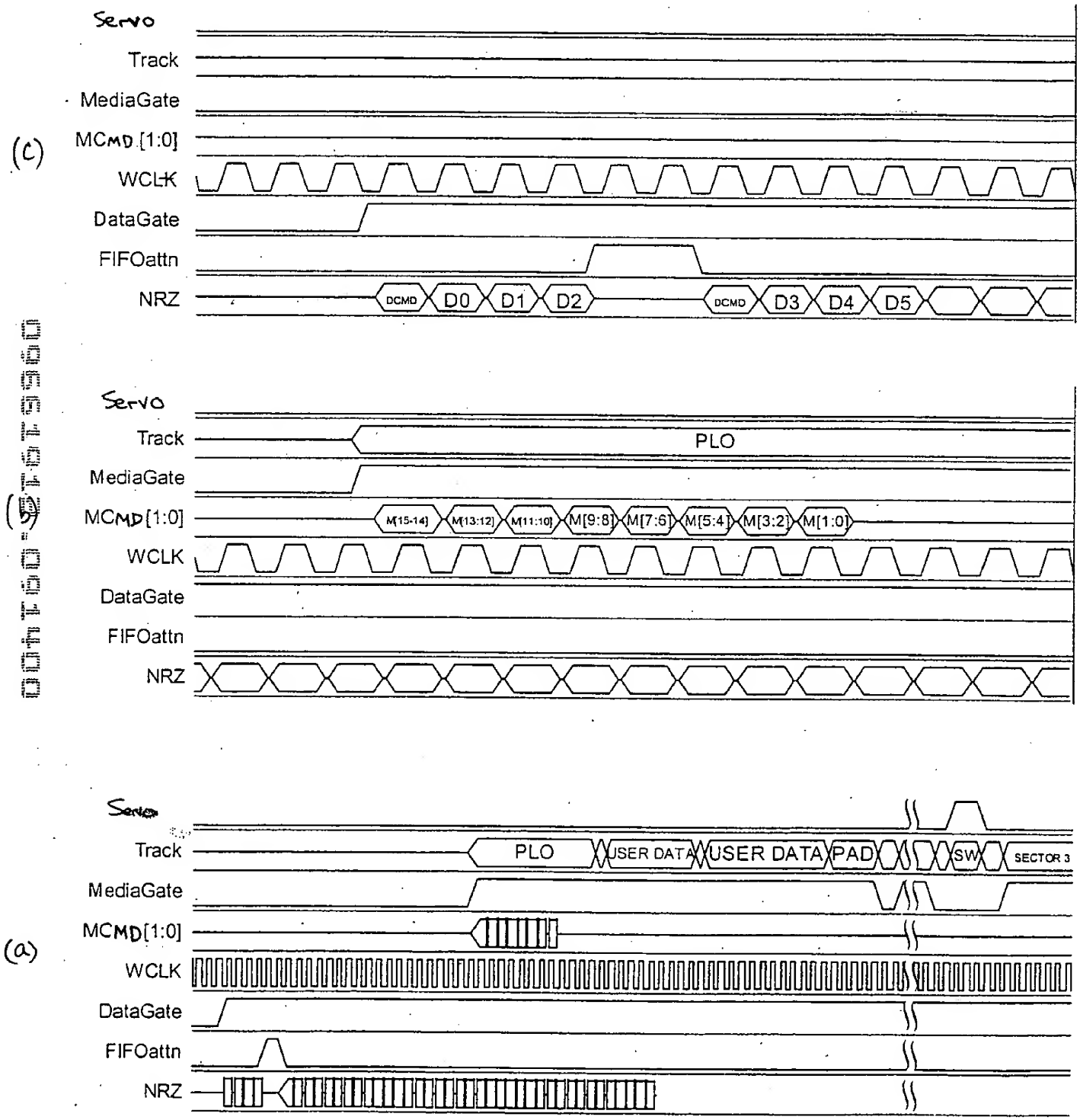

Fig. 4

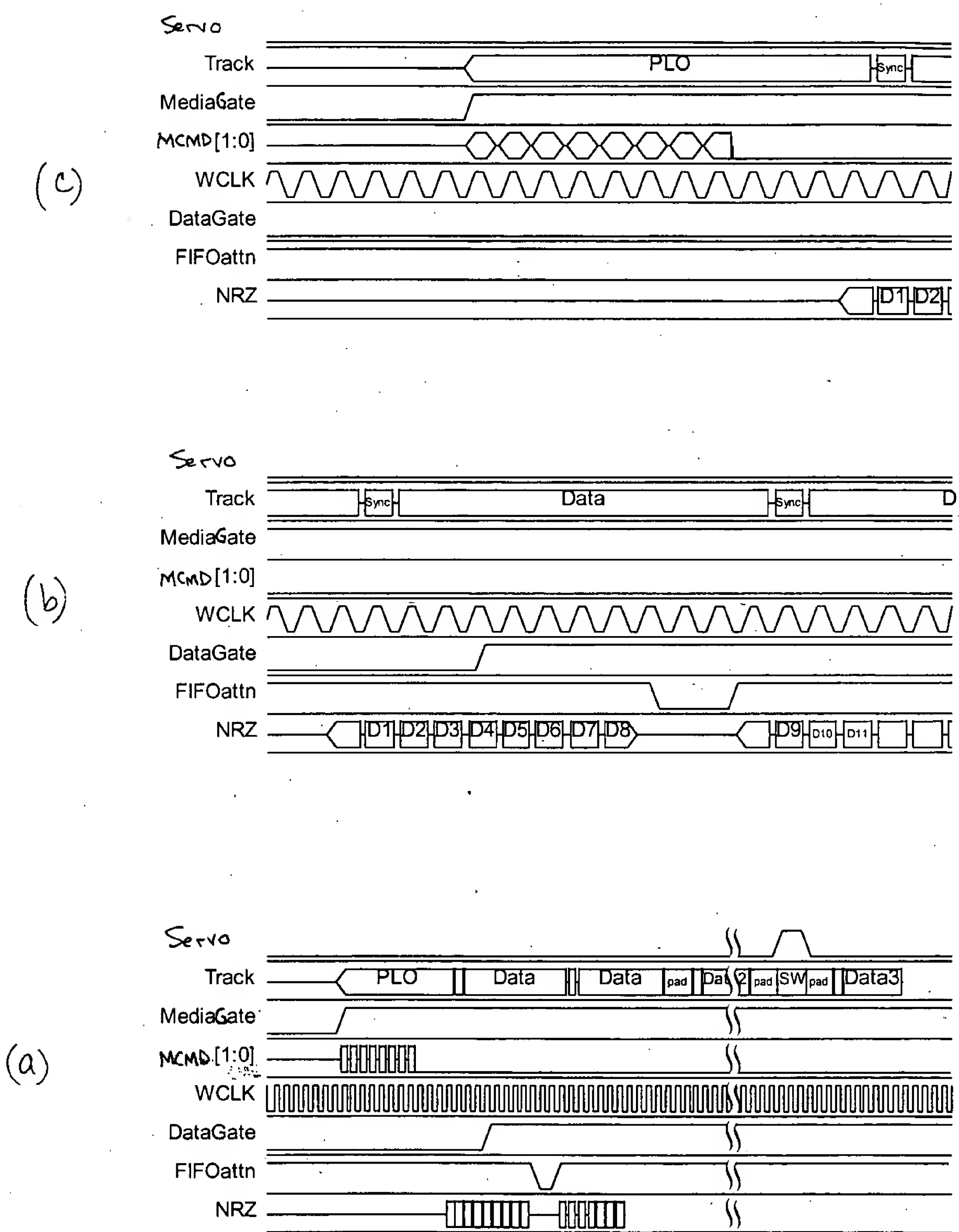
(c)
Servo
Track
MediaGate
MCMD[1:0]
WCLK
DataGate
FIFOattn
NRZ
PLO
Sync
D1
D2
(b)
Servo
Track
MediaGate
MCMD[1:0]
WCLK
DataGate
FIFOattn
NRZ
Sync
Data
Sync
D
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
(a)
Servo
Track
MediaGate
MCMD[1:0]
WCLK
DataGate
FIFOattn
NRZ
PLO
Data
Data
pad
pad
SW
pad
Data3

Fig. 5